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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,378	08/17/2001	Serge Lasserre	TI-32234	4429

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	5

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,378	LASSERRE ET AL.	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 15, paragraph 30 makes reference Fig. 6 concerning an instruction cache "106" (line 4 of paragraph 30) and a data cache "102" (lines 4 and 7 of paragraph 30). It is believed that these references in the specification should be instruction cache "206" and data cache "202" from Fig. 6. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 1, the specification makes reference to a US Patent Application but no serial number is provided.

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 2 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 2 recites the limitation "The identifier value" in line 1. There is insufficient antecedent basis for this limitation in the claim. It is believed that the problem of the claim is caused by the claim being dependent upon itself. The examiner interprets the claim as being dependent upon claim 1 and it will be treated as such for the purposes of further examination.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-7 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kakeda et al., U.S. Patent 6,564,311, hereinafter referred to as "Kakeda".

10. Referring to claim 1, Kakeda teaches a method of operating a digital system having a processor and memory (See Fig. 1). Kakeda teaches the system containing an address translating apparatus that contains a plurality of entries, which is interpreted as requesting memory transactions. The entries contain page numbers and a process identifier that is composed of plural bits (See Col. 3, lines 37-42). The process identifier is interpreted as an identifier indicating a task, and the process identifier having plural bits is interpreted as the processor executing a plurality of tasks. Kakeda discloses checking global bits to determine if a comparison is needed between the current process id and the stored process id, the checking of the global bits is interpreted as detecting an error condition because the global bits act as error flags. The global bits help determine sharing of the virtual space and an access by a different process can cause unwanted modification (See Col. 2, lines 43-52 and Col. 4, lines 53-65). Finally

Kakeda teaches comparing the process id of the current running process with the stored process id when it is determined to be needed by the global bits for allowing access to the memory transaction, the comparing of the process identifiers is interpreted as recovering from the error condition using the identifier value of the memory transaction to identify the task being the source of the transaction and thus having access to it (See Col. 4, lines 53-65).

11. Referring to claim 2, Kakeda teaches the identifier being a process identifier, which is interpreted to be a task identifier (See Col. 3, lines 40-41).

12. Referring to claim 3, Kakeda teaches the identifier being a process identifier (See Col. 3, lines 40-41). The process identifier identifies the process or particular running environment on the processor, this is interpreted as being a resource of the computer system and thus being a resource identifier.

13. Referring to claim 4, Kakeda teaches comparing a current process identifier with a stored process identifier (See Col. 4, lines 53-65). The is interpreted as the stored process identifier being identifier of a previous process that is currently in a wait state and not executing thus the transaction having been delayed.

14. Referring to claim 5, Kakeda discloses the buffer containing both the virtual page number, or transaction address, and the identifier value (See Fig. 4 and Col. 3, lines 40-41).

15. Referring to claim 6, Kakeda discloses the buffer contain both the virtual page number, or transaction address, and the identifier value (See Fig. 4 and Col. 3, lines 40-41). Since both values are stored together, it is interpreted as the values being kept coherent with the access to memory provided by the virtual page number.

16. Referring to claim 7, Kakeda discloses the memory transaction being a request from the CPU to main memory with the help of a TLB (See Col. 1, lines 46-55). A memory access to main memory from the CPU will result in a cache load.

17. Referring to claim 10, Kakeda teaches the mode of the global bits requiring a perfect match of the process identifiers (See Col. 6, lines 61-67). This is interpreted as not allowing access to a mismatch and thus stopping or suspending the process or task attempting access the memory.

18. Referring to claim 11, Kakeda teaches a digital system having a processor and memory (See Fig. 1). Kakeda teaches the system containing an address translating apparatus that contains a plurality of entries, which is interpreted as identifier circuitry. The entries contain page numbers and a process identifier that is composed of plural

bits (See Col. 3, lines 37-42). The process identifier is interpreted as an identifier indicating a task, and the process identifier having plural bits is interpreted as the processor executing a plurality of tasks. Kakeda discloses comparison information storage means, which is interpreted as abort circuitry, checking global bits to determine if a comparison is needed between the current process id and the stored process id, the checking of the global bits is interpreted as detecting an error condition because the global bits act as error flags. The global bits help determine sharing of the virtual space and an access by a different process can cause unwanted modification (See Col. 2, lines 43-52 and Col. 4, lines 53-65). Finally Kakeda teaches comparing the process id of the current running process with the stored process id when it is determined to be needed by the global bits for allowing access to the memory transaction, the comparing of the process identifiers is interpreted as recovering from the error condition using the identifier value of the memory transaction to identify the task being the source of the transaction and thus having access to it (See Col. 4, lines 53-65).

19. Referring to claim 12, Kakeda teaches the digital system having a translation look-aside buffer that holds identifier values and virtual page numbers, interpreted as transaction addresses (See Col. 3, lines 36-41).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakeda in view of Gunji, U.S. Patent 5,487,154.

22. Referring to claim 8, Kakeda teaches all the limitations (See rejection of claim 1) except for the memory transaction request being from a direct memory access engine. Gunji teaches a DMA being used for data reception and transmission to memory (See Fig. 4 and Col. 3, lines 25-26). It would be obvious to one of ordinary skill in the art at the time of the invention to use the DMA of Gunji for the memory transactions of Kakeda. This would have been obvious to one of ordinary skill in the art at the time of the invention because the DMA alleviates burden placed upon the processor (See Gunji, Col. 3, lines 27-31).

23. Referring to claim 9, Kakeda discloses all the limitations (See rejection of claim 1) except for the memory transaction request being from a co-processor. Gunji teaches a DMA being used for data reception and transmission to memory (See Fig. 4 and Col. 3, lines 25-26). The DMA is interpreted as a specialized processor or "co-processor" used for memory transactions. It would be obvious to one of ordinary skill in the art at the time of the invention to use the DMA of Gunji for the memory transactions of Kakeda. This would have been obvious to one of ordinary skill in the art at the time of

the invention because the DMA alleviates burden placed upon the processor (See Gunji, Col. 3, lines 27-31).

24. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakeda in view of Singh, U.S. Patent 6,389,447.

25. Referring to claim 13, Kakeda teaches all the limitations (See rejection of claim 12) except system being in a PDA that includes a display, RF circuitry, and an aerial connected to the RF circuitry. Singh discloses task management system for a handheld computer, interpreted as a PDA (See Col. 1, lines 23-39). The device has a display, transmitter and receiver circuitry, interpreted as RF circuitry, and an antenna or aerial (See Fig. 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the PDA of Singh with the digital system of Kakeda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the digital system of Kakeda provides identification of tasks and a PDA that runs more than one task needs to keep track of all the tasks with out user invention since the PDA is unable to display all tasks on its small screen (See Singh, Col. 1, lines 23-39).

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are examples of closely related process or task managing systems.

U.S. Patent 6,219,689 to Mori

U.S. Patent 5,463,733 to Forman et al.

U.S. Patent 6,253,225 to Nakahara et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM

April 14, 2004

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